

REMARKS

Introduction

Claims 1-5, 7, 8, 10 and 11 remain in the application, of which claims 1 and 5 are in independent form. Claims 5, 7 and 10 have been amended. Claims 6 and 9 have been cancelled.

Non-Statutory Double Patenting Rejections

Claims 1-11 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7 of copending U.S. Patent Application No. 10/540,702, which is presently under examination and has not yet been allowed.

Applicants acknowledge the provisional non-statutory double patenting rejection set forth in the Office Action. By this Amendment, applicants address the other rejections and objections set forth in the Office Action. Applicants respectfully defer discussion of the provisional non-statutory double patenting rejections to a later date, as necessary.

Rejections under 35 U.S.C. § 103(a)

Claims 1-3, 5, 6 and 9-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over International Patent Publication WO 01/73566 A2 (*Wertheim*) in view of applicants' admitted prior art (AAPA).

Claim 1 of the present application is directed to a "clustered Instruction Level Parallelism processor." The clustered Instruction Level Parallelism processor comprises a "plurality of clusters" with each cluster comprising "at least one register file and at least one functional unit." The clustered Instruction Level Parallelism processor also includes a "bus for connecting said clusters, said bus means comprising a plurality of bus segments, and switching

means, arranged between adjacent bus segments, for connecting or disconnecting adjacent bus segments."

Wertheim is directed to dynamic bus partitioning for electronic circuits to reduce power consumption. See *Wertheim* at Abstract. The described electronic circuit is a digital signal processor (DSP) having computational blocks, a memory and a control block constituting a core processor. See *Id.* at FIG. 1 and first paragraph of detailed description.

As conceded by the Examiner, *Wertheim* does not describe clusters comprising "at least one register file and at least one functional unit," as claimed by the present application. In addition, *Wertheim* is directed to electronic circuits such as digital signal processors, and does not describe a "clustered Instruction Level Parallelism processor," as claimed by the present application.

Applicants submit that neither AAPA nor *Wertheim* teach, suggest, or provide motivation for applicants' claimed invention. In contrast, applicants submit that the § 103 rejections to the claims are not supported by evidence of motivation. The claimed invention is directed to a "clustered Instruction Level Parallelism processor" having clusters, with each cluster comprising "at least one register file and at least one functional unit." As described in the present application as filed, the use of a "bus for connecting said clusters" having "a plurality of bus segments, and switching means, arranged between adjacent bus segments, for connecting or disconnecting adjacent bus segments," provides that "data moves between local or adjacent clusters can have lower latencies than moves over a different bus segment, i.e., over different switches." *Present Application* as filed at page 3, lines 22-25. Thus, the claimed invention is directed at problems of latency and scalability related to Instruction Level Parallelism processors, and seeks to provide a solution to these difficulties by "improving bandwidth of a bus

within an ICC scheme for a clustered ILP processor, while decreasing the latency of said bus."
Id. at page 3, lines 5-6.

In contrast, as described above, *Wertheim* is not directed to Instruction Level Parallelism processors, and thus does not describe cluster comprising "at least one register file and at least one functional unit." Moreover, as also described above, *Wertheim* is directed to reduced power consumption, and not the latency difficulties often encountered with Instruction Level Parallelism processors. Accordingly, applicants submit that the combination of AAPA and *Wertheim* is improper, and the combination does not teach, suggest, or provide motivation for the claimed invention.

Accordingly, for at least these reasons, claim 1 is deemed to distinguish patentably over *Wertheim* in view of AAPA

Claims 2 and 3 depend from claim 1. Accordingly, each of claims 2 and 3 is deemed allowable, at least for the reasons stated above with respect to claim 1.

Amended claim 5 is not taught or suggested by *Wertheim* at least because amended claim 5 recites

opening/closing said switching means according to said transfer word; wherein said transfer word represents the sending direction for sending operation and the receiving direction for the receiving operation; and

wherein said sending direction or said receiving direction is left, right or all.

Wertheim does describe the opening of switches, but *Wertheim* does not teach or suggest a method wherein "said transfer word represents the sending direction for sending operation and the receiving direction for the receiving operation; and wherein said sending direction or said receiving direction is left, right or all." In fact, the architectures shown by *Wertheim* teach away from a "left, right or all system due to the non-linear alignment of components. (See *Wertheim* at FIGs. 3 and 4).

AAPA does not cure the deficiencies of *Wertheim*.

Each of claims 10 and 11 depend from claim 5. Accordingly, each of claims 10 and 11 is deemed allowable, at least for the reasons stated above with respect to claim 5.

Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Wertheim* in view of applicants' admitted prior art (AAPA) and further in view of U.S. Patent Publication No. 2001/0054124 (*Tsurta*).

As described above, neither *Wertheim* nor AAPA, either taken alone, or in combination, teach, suggest, or provide motivation for the invention recited by claim 1. Claim 4 depends from claim 1, and is thus patentable over any *Wertheim*-AAPA combination for at least the reasons described above with respect to claim 1. *Tsurta* does not cure the deficiencies of *Wertheim* and AAPA. While *Tsurta* does describe a processor system having multiple busses, the configuration of the multiple busses in *Tsurta* is similar to that described in the prior art. Accordingly, applicants submit that any *Wertheim*-AAPA-*Tsurta* combination does not teach, suggest or provide motivation for the invention of claim 4 of the present application, and withdrawal of the rejection is requested.

Claims 7 and 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Wertheim* in view of applicants' admitted prior art (AAPA) and further in view of "Resource Allocation in a Dynamically Partitionable Bus Network Using a Graph Coloring Algorithm" (*Woo*).

As described above, neither *Wertheim* nor AAPA, either taken alone, or in combination, teach, suggest, or provide motivation for the invention recited by claim 5. Claims 7 and 8 depend from claim 5, and are thus patentable over any *Wertheim*-AAPA combination for at least the reasons described above with respect to claim 5. *Woo* does not cure the deficiencies of *Wertheim* and AAPA. While *Woo* does describe switching information paths to allocate

network resources in a dynamically partitionable bus network, the proposed *Wertheim-AAPA-Woo* combination does not teach, suggest, or provide motivation for the combination of features described above with respect to claim 5, from which claims 7 and 8 depend. Accordingly, applicants submit that any *Wertheim-AAPA-Woo* combination does not teach, suggest or provide motivation for the inventions of claims 7 and 8 of the present application, and withdrawal of the rejections is requested.

Thus, applicants submit that each of the claims of the present application are patentable over each of the references of record, either taken alone, or in any proposed hypothetical combination. Accordingly, withdrawal of the rejections to the claims is respectfully requested.

Conclusion

In view of the above remarks, reconsideration and allowance of the present application is respectfully requested.

Respectfully submitted,

Paul Im
Registration No. 50,418

/ James Dobrow /
By: James Dobrow
Attorney for Applicants
Registration No. 46,666

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Mail all correspondence to:

Paul Im, Registration No. 50,418
US PHILIPS CORPORATION
P.O. Box 3001
Briarcliff Manor, NY 10510-8001
Phone: (914) 333-9627
Fax: (914) 332-0615